

## **REMARKS**

Please reconsider the present application in view of the above amendments and the following remarks. Applicant thanks the Examiner for carefully considering the present application.

### **I. Disposition of Claims**

Claims 1-13 are currently pending in the present application. By way of this reply, claims 1, 6, 7, 9, 10, and 13 have been amended and claim 8 has been canceled without prejudice or disclaimer.

### **II. Claim Amendments**

Claim 1 has been amended to recite that at least one of the high comparator output and the low comparator output clock the circuit referred to in claim 1. No new matter has been added by way of this amendment as support for this amendment may be found, for example, in Figure 1 of the present application.

Claim 7 has been amended to recite that the plurality of flip-flop circuits of the high-to-low sub-circuit are clocked by at least one of the output of the high comparator and the output of the low comparator. Further, claim 7 has been amended to recite that the plurality of flip-flop circuits of the low-to-high sub-circuit are clocked by at least one of the output of the high comparator and the output of the low comparator. No new matter has been added by way of these amendments as support for these amendments may be found, for example, in Figure 1 of the present application.

Claim 9 has been amended to recite that the activating of an alarm if a high signal

voltage is less than a high voltage limit is dependent on being clocked by a first signal generated dependent on comparing the high signal voltage with the high voltage limit. Further, claim 9 has been amended to recite that the activating of an alarm if a low signal voltage is greater than a low voltage limit is dependent on being clocked by a second signal generated dependent on comparing the low signal voltage with the low voltage limit. No new matter has been added by way of these amendments as support for these amendments may be found, for example, in Figure 1 of the present application.

Claim 13 has been amended to recite that a plurality of flip-flop circuits of the low-to-high circuit are clocked by a signal generated dependent on the comparing of a high signal voltage with a high voltage limit. Further, claim 13 has been amended to recite that a plurality of flip-flop circuits of the high-to-low circuit are clocked by a signal generated dependent on the comparing of a low signal voltage with a low voltage limit. No new matter has been added by way of these amendments as support for these amendments may be found, for example, in Figure 1 of the present application.

Further, claims 6, 7, and 10 have been amended to replace the instances of “300 mV” with “substantially 300 mV.” No new matter has been added by way of these amendments.

### **III. Objection(s)**

The Abstract was objected to as being too short. By way of this reply, the Abstract has been amended to be longer and more descriptive of the present invention. Accordingly, withdrawal of the objection to the Abstract is respectfully requested.

#### **IV. Rejection(s) Under 35 U.S.C § 102**

Claims 1-13 of the present application were rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,790,613 issued to Tateishi (hereinafter "Tateishi"). For the reasons set forth below, this rejection is respectfully traversed.

The present invention is directed to a technique for performing a self-diagnosis of signal noise error. With reference to the exemplary embodiment of the present invention shown in Figure 2 of the present application, a noise margin self-diagnostic receiver circuit in accordance with the present invention includes (1) a high comparator **58** that generates an output dependent on a comparison of a signal-of-interest with a high voltage limit, (2) a low comparator **60** that generates an output dependent on a comparison of the signal-of-interest with a low voltage limit, and (3) circuitry clocked by at least one of the high comparator output and the low comparator output, where the circuitry indicates if a particular noise error on the input signal is detected. Figure 2 of the present application shows that the outputs of the high and low comparators **58**, **60** are connected to the clock inputs of the flip-flops **62a**, **62b**, **62c**, **62d**. These flip-flops **62a**, **62b**, **62c**, **62d** are used to process the outputs of the high and low comparators **58**, **60** in order to generate/activate an alarm indicative of noise error on the signal-of-interest.

Accordingly, independent claims 1, 7, 9, and 13 require in some form that the circuitry or method used to activate or generate an alarm indicative of noise error be clocked by signals generated dependent on at least one a comparison of a signal-of-interest with a high voltage limit and a comparison of the signal-of-interest with a low voltage limit.

Tateishi, in contrast to the present invention, fails to disclose all the limitations

recited in amended independent claims 1, 7, 9, and 13 of the present application. For example, as disclosed in Figures 5, 8-10, and 13-15 of Tateishi, Tateishi shows that the output of the purported high comparator **8U1** and the output of the purported low comparator **8L1** are connected to data inputs of flip-flops **8U2**, **8L2**. Thus, in Tateishi, a signal generated dependent on a comparison of the signal-of-interest **PE** to either a high voltage limit (by purported high comparator **8U1**) or a low voltage limit (by purported low comparator **8L1**) is not used to clock any circuitry at all. Accordingly, Tateishi fails to disclose at least those limitations of amended independent claims 1, 7, 9, and 13 related to the clocking of circuitry by signals generated dependent on a comparison of a signal-of-interest to either a high voltage limit or a low voltage limit.

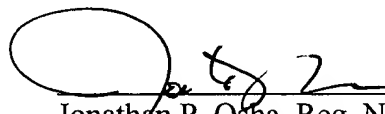
In view of the above, Tateishi fails to show or suggest the present invention as recited in amended independent claims 1, 7, 9, and 13 of the present application. Thus, amended independent claims 1, 7, 9, and 13 of the present application are patentable over Tateishi. Dependent claims are allowable for at least the same reasons. Accordingly, withdrawal of this rejection is respectfully requested.

**V. Conclusion**

Applicant believes this reply is fully responsive to all outstanding issues and places this application in condition for allowance. If this belief is incorrect, or other issues arise, the Examiner is encouraged to contact the undersigned or his associates at the telephone number listed below. Please apply any charges not covered, or any credits, to Deposit Account 50-0591 (Reference Number 06145.003001;P4928).

Respectfully submitted,

Date: 1/28/04

  
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